In the Claims:

1. (previously presented) A microcontroller circuit comprising:

a bus;

a microprocessor coupled to said bus;

a memory coupled to said bus, wherein said memory comprises a non-volatile memory; and

a plurality of functional units coupled to said bus, wherein said non-volatile memory functions to program said functional units and wherein said plurality of functional units comprise:

an interconnect wherein said interconnect is dynamically configurable and programmable;

an analog functional block coupled to said interconnect wherein said analog function block is dynamically configurable and programmable to perform one or more of a plurality of various analog functions; and

a dynamically configurable and programmable digital functional block coupled to said interconnect, wherein said dynamically configurable and programmable digital functional block is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation.

2. (Previously Presented) The microcontroller circuit as recited in Claim 1, wherein said memory comprises an erasable memory.

3. (previously presented) The microcontroller circuit as recited in Claim 1, wherein said functional units further comprise a programmable input/output coupling.

4. (previously presented) The microcontroller circuit as recited in Claim 1, wherein a component of said circuit is dynamically programmable according to an user input.

5. (Previously Presented) The microcontroller circuit as recited in Claim 4, wherein said component is selected from the list consisting of said interconnect, said analog functional block, and said digital functional block.

6. (Previously Presented) The microcontroller circuit as recited in Claim 5, wherein a function of said circuit is programmable.

7. (Previously Presented) The microcontroller circuit as recited in Claim 6, wherein said function corresponds to a configuration state.

8. (Previously Presented) The microcontroller circuit as recited in Claim 7, wherein said configuration state is configured according to said user input.

9. (Previously Presented) The microcontroller circuit as recited in Claim 1, wherein said memory further comprises a random access memory.

10. (Previously Presented) The microcontroller circuit as recited in Claim 1, wherein said non-volatile memory comprises a programmable memory.

11. (previously presented)An integrated circuit comprising:

a bus;

a microprocessor coupled to said bus;

a memory coupled to said bus, wherein said memory comprises a non-volatile memory;

a plurality of functional units coupled to said bus, wherein said non-volatile memory stores code for programming said functional units and wherein said plurality of functional units comprise:

an interconnect wherein said interconnect is dynamically configurable and programmable;

an analog functional block coupled to said interconnect wherein said analog function block is dynamically configurable and programmable to perform one or more of a plurality of various analog functions; and

a dynamically configurable and programmable digital functional block coupled to said interconnect, wherein said dynamically configurable and programmable digital functional block is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation; and

an input/output coupling, wherein said integrated circuit comprises a microcontroller.

12. (Canceled)

13. (Original) The circuit as recited in Claim 11, wherein said programmable component is programmable according to a user input.

14. (Original) The circuit as recited in Claim 13, wherein a function of said circuit is programmable.

15. (Original) The circuit as recited in Claim 14, wherein said function corresponds to a configuration state.

16. (Original) The circuit as recited in Claim 15, wherein said configuration state is configured according to said user input.

17. (Previously Presented) A microcontroller circuit, comprising:

a microprocessor;

a plurality of analog circuit blocks wherein said analog function block is dynamically configurable and programmable to perform one or more of a plurality of various analog functions;

a plurality of dynamically programmable digital circuit blocks wherein at least one of said dynamically programmable digital circuit blocks is coupled directly or indirectly to at least one of said dynamically programmable analog circuit blocks wherein at least a first one of said dynamically programmable digital circuit blocks is coupled directly or indirectly to at least a first one of said dynamically programmable analog circuit blocks, and at least a second one of said dynamically programmable digital circuit blocks and said dynamically programmable analog circuit blocks is coupled directly or indirectly to said microprocessor and wherein said coupling is achieved with an interconnect, wherein said interconnect is dynamically programmable and configurable, wherein each dynamically programmable digital circuit block is configurable to perform any one of a plurality of digital functions upon being configured with a single register write operation; and

a programmable non-volatile memory coupled directly or indirectly to said plurality of dynamically programmable digital circuit blocks and said plurality of dynamically programmable analog circuit blocks, said programmable non-volatile memory storing code for programming at least one of said programmable digital circuit blocks and at least one of said plurality of programmable analog circuit blocks.

18. (Previously Presented) The microcontroller circuit as recited in Claim 17, wherein each of said plurality of dynamically programmable digital circuit blocks is dynamically configured to provide at least one of said digital functions.

19. (Canceled)

20. (Previously Presented) The microcontroller circuit as recited in Claim 17, wherein at least a third one of said programmable digital circuit blocks is coupled to a fourth one of said programmable digital circuit blocks, and at least a third one of said programmable analog circuit blocks is coupled to a fourth one of said programmable analog circuit blocks.

21. (Previously Presented) The microcontroller circuit as recited in Claim 20, wherein a programmed combination of said plurality of programmable digital circuit blocks and said programmable analog circuit blocks is configured to provide at least one digital and/or analog system function.

22. (Canceled)

23. (Previously Presented) The microcontroller circuit as recited in Claim 17, wherein said programmable memory comprises an erasable and programmable memory.

24. (Previously Presented) The microcontroller circuit as recited in Claim 23, wherein said programmable memory comprises an electrically erasable and programmable memory.

25. (Previously Presented) The microcontroller circuit as recited in Claim 17, further comprising a plurality of dynamically programmable and configurable input and/or output blocks, coupled directly or indirectly to at least one of said programmable memory, said programmable digital circuit blocks, said plurality of programmable analog circuit blocks, and said microprocessor.

26. (Previously Presented) The microcontroller circuit as recited in Claim 25, wherein at least a first one of said plurality of dynamically programmable and configurable input and/or output blocks couples one or more external signals to said microprocessor.

27. (Previously Presented) The microcontroller circuit as recited in Claim 26, wherein at least a second one of said plurality of dynamically programmable and configurable input and/or output blocks couples one or more external signals to at least one of said programmable digital circuit blocks and said plurality of programmable analog circuit blocks.

28. (Previously Presented) The microcontroller circuit as recited in Claim 27, wherein at least said second one of said plurality of dynamically programmable and configurable input and/or output blocks couples one or more external signals to at least one of said plurality of programmable analog circuit blocks.

29. (Previously Presented) The microcontroller circuit as recited in Claim 28, wherein said at least one of said plurality of programmable analog circuit blocks send signals to at least one of said programmable digital circuit blocks.

30. (Previously Presented) The microcontroller circuit as recited in Claim 27, wherein at least a third one of said plurality of input and/or output blocks sends data to said programmable memory.

31. (Previously Presented) The microcontroller circuit as recited in Claim 27, further comprising a plurality of registers configured to store programming data for said plurality of programmable digital circuit blocks.

32. (Previously Presented) The microcontroller circuit as recited in Claim 27, further comprising a plurality of latches configured to store programming data for said plurality of programmable analog circuit blocks.

33. (Previously Presented) The microcontroller circuit as recited in Claim 27, further comprising a global routing matrix configured to couple said plurality of input and/or output blocks to said plurality of programmable digital circuit blocks and said plurality of programmable analog circuit blocks.

34. (Previously Presented) The microcontroller circuit as recited in Claim 27, further comprising a system macro routing matrix configured to couple a subset of said plurality of programmable digital circuit blocks to a subset of said plurality of programmable analog circuit blocks.

35. (Previously Presented) A microcontroller circuit, comprising:

a plurality of input and/or output blocks;

a plurality of programmable analog circuit blocks, wherein said analog circuit blocks are dynamically configurable and programmable to perform one or more of a plurality of various analog functions; and

a plurality of dynamically programmable digital circuit blocks, at least one of said programmable digital circuit blocks being coupled directly or indirectly to at least one of said programmable analog circuit blocks wherein at least one of said programmable digital circuit blocks and said programmable analog circuit blocks is coupled directly or indirectly to at least one of said input and/or output blocks, wherein each dynamically programmable digital circuit block is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation; and

a programmable non-volatile memory coupled to said plurality of programmable digital circuit blocks and said plurality of programmable analog circuit blocks, said programmable memory comprising data for programming at least one of said programmable digital circuit blocks and at least one of said plurality of programmable analog circuit blocks.

36. (Previously Presented) The circuit as recited in Claim 35, wherein at least a first one of said plurality of input and/or output blocks sends signals to at least a first one of said plurality of programmable analog circuit blocks, said first programmable analog circuit block sends signals to at least a first one of said plurality of programmable digital circuit blocks, and said first programmable digital circuit block sends signals to a same or different one of said plurality of input and/or output blocks.

37. (Previously Presented) A microcontroller circuit, comprising:

a programmable non-volatile memory containing programming code;

a plurality of dynamically programmable analog circuit blocks configured to receive a first subset of said programming data from said programmable memory and wherein said analog circuit blocks are dynamically configurable and programmable to perform a plurality of various analog functions; and

a plurality of dynamically programmable digital circuit blocks configured to receive a second subset of said programming data from said programmable memory, at least a first one of said programmable digital circuit blocks being coupled directly or indirectly to at least a first one of said programmable analog circuit blocks, wherein each dynamically programmable digital circuit block is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation.

38. (Previously Presented) The circuit as recited in Claim 37, wherein a second one of said plurality of programmable analog circuit blocks is coupled to at least one of said first programmable analog circuit block and a second one of said plurality of programmable digital circuit blocks.

39. (Previously Presented) The circuit as recited in Claim 37, wherein a second one of said plurality of programmable digital circuit blocks is coupled to at least one of said first programmable digital circuit block and a second one of said plurality of programmable analog circuit blocks.

40. (Previously Presented) The circuit as recited in Claim 38, wherein said second programmable analog circuit block is coupled to said first programmable analog circuit block and second one of said plurality of programmable digital circuit blocks is coupled to said first programmable digital circuit block.

41. (Previously Presented) The circuit as recited in Claim 38, wherein said second programmable analog circuit block is coupled to said second programmable digital circuit block.

42. (currently amended) A microcontroller circuit, comprising:

a plurality of analog circuit blocks wherein said analog circuit blocks are dynamically programmable and configurable to perform one or more of a plurality of

various analog functions and wherein said plurality of programmable analog circuit blocks comprises a matrix of n by m analog configurable system macros, n and m independently being an integer of at least two;

a plurality of programmable digital circuit blocks configured to provide at least one of a plurality of digital functions, wherein each programmable digital circuit block is configurable to perform any one of said digital functions upon being configured with a single register write operation;

a routing matrix configured to couple a subset of said plurality of programmable analog circuit blocks to a first subset of said plurality of programmable digital circuit blocks, at least a first one of said programmable analog circuit blocks being coupled to at least a first one of said programmable digital circuit blocks; and

a programmable non-volatile memory coupled directly or indirectly to said plurality of programmable digital circuit blocks and said plurality of programmable analog circuit blocks, said programmable memory comprising data for programming at least one of said programmable digital circuit blocks and at least one of said plurality of programmable analog circuit blocks.

43. (Previously Presented) The circuit as recited in Claim 42, wherein when programmed, each of said plurality of programmable analog circuit blocks provides at least one of said plurality of analog functions.

44. (Previously Presented) The circuit as recited in Claim 42, wherein when programmed, each programmable digital circuit blocks provides at least one of said digital functions.

45. (Previously Presented) The circuit as recited in Claim 43, wherein when programmed, said plurality of programmable analog circuit blocks and said plurality of programmable digital circuit blocks provides at least one digital and/or analog function.

46. (Previously Presented) The circuit as recited in Claim 42, wherein when programmed, said routing matrix couples a second one of said subset of said plurality of programmable analog circuit blocks to a second one of said subset of said plurality of programmable digital circuit blocks.

47. cancelled)

48. (currently amended) The circuit as recited in Claim [[47]] 42, wherein each of said analog configurable system macros is configured to provide one or more analog functions selected from the group consisting of a gain function, a comparator function, a switched capacitor function, a filter function, an analog to digital conversion function, a digital to analog conversion function, and an amplifier function.

49. (Previously Presented) The circuit as recited in Claim 42, wherein at least two of said plurality of programmable digital circuit blocks are coupled in series to provide a digital system function.

50. (Canceled)

51. (Previously Presented) A programmable digital circuit in a microcontroller comprising a non-volatile memory and a programmable analog circuit dynamically programmable to perform one or more of a plurality of various analog functions wherein said non-volatile memory stores code for programming said digital and said analog circuit, said programmable digital circuit comprising at least three programmable digital circuit blocks coupled in series and/or in parallel, each programmable digital circuit block being (i) controlled by an n bit register or look up table containing programming information including a cascading bit and (ii) configured to provide at least one of a plurality of digital functions, wherein the cascading bit determines whether a particular programmable digital circuit block is coupled is series with an adjacent programmable digital circuit block, and when programmed, the programmable digital circuit provides at least one digital system function, wherein each programmable digital circuit block is configurable to perform any one of said digital functions upon being configured with a single register write operation.

52. (Previously Presented) A system comprising:

a microcontroller comprising a non-volatile memory;

a subsystem comprising an array of digital components and an array of analog components wherein said analog components are programmable to perform one or more of a plurality of various analog functions and wherein said analog components and said digital components are programmed with code stored in said non-volatile memory, wherein each digital component is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation; and

a coupling mechanism coupled to said subsystem; wherein selectively, said functionality is configurable to execute a first function according to an input of a first type, said coupling mechanism is configurable to implement a connectability state for said system with which said system is connectable to an external entity according to a user input of a second type.

53-56. (Canceled)

57. (Previously Presented) The system as recited in Claim 52, further comprising a timing functionality, which is configurable to generate a plurality of time bases according to a user input of a third type.

58. (Previously Presented) In a system disposed in an integrated circuit, said system comprising:

a microcontroller comprising a non-volatile program memory;

a subsystem coupled to said non-volatile program memory, comprising a plurality of analog functionalities and of digital functionalities that are both configurable according to a user input wherein said analog functionalities are programmable to perform one or more of a plurality of various analog functions and wherein said analog functionalities and said digital functionalities are programmed with code stored in said non-volatile program memory, wherein each digital functionality is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation;

an interconnecting mechanism configurable for selectively interconnecting said plurality of analog functionalities and said plurality of digital functionalities according to said user input; and

a coupling mechanism coupled to said subsystem that is configurable to implement a connectability state for said system by which said system is connectable to an external entity according to said user input, a method of configuring said system comprising:

a) selecting a function from the list consisting of analog functions, digital functions, and; mixed analog and digital functions

b) selecting an interconnection state to effectuate an interconnection between said analog functionalities and said digital functionalities corresponding to said function;

c) selecting said connectability state to effectuate an connection between said system and an external entity corresponding to said function; and

d) implementing said function, said interconnection state, and said connectability state according to said a), said b) and said c).

59. (Original) The method as recited in Claim 58, wherein said system further comprises a timing functionality configurable to generate a plurality of time bases, said method further comprising:

selecting a timing base from said plurality of timing bases; and

implementing said timing base accordingly.